

National Aeronautics and Space Administration



Sensors

Active Pixel Sensor Design and Operation

A complementary metal oxide semiconductor active pixel sensor for image acquisition

NASA's Jet Propulsion Laboratory has developed an imaging device called an active pixel sensor that is inexpensive and easy to fabricate. The active pixel sensor is designed to perform at least as well as conventional charge coupled device (CCD) imagers without all the drawbacks. CCD imagers are susceptible to radiation damage, require good light shielding to avoid smear, and have high power dissipation for large arrays. In addition, the CCD fabrication process is incompatible with complementary metal oxide semiconductor (CMOS) processing, which makes it difficult to integrate on-chip signal processing electronics. JPL's active pixel sensor, which can be fabricated using an industry-standard CMOS-compatible process and smaller-sized pixels, is an integrated imaging device that is well-suited for a variety of applications.

BENEFITS

- Integrated, on-chip signal processing is cheaper and more efficient
- A transparent refractive microlens layer focuses light onto the photosensors
- A column-parallel array structure improves the resolution of each pixel
- Non-destructive readout capability is ideal for low-light imaging applications

technology solution

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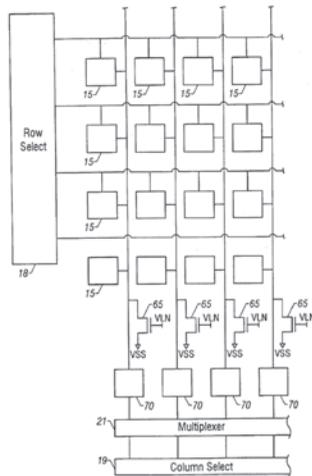
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THE TECHNOLOGY

JPL's active pixel imaging device comprises a focal plane array having a simple floating gate (SFG) pixel structure and a readout circuit. An SFG sensor array can be implemented using an industry-standard CMOS-compatible fabrication process, allowing the readout circuitry to be implemented as inexpensive CMOS circuits. A column-parallel approach—in which an entire row of the array is processed simultaneously—frees up additional photosensitive cell area and thus improves resolution. In addition to a transparent refractive microlens layer, which can be contoured to focus light toward the center of each photogate, an optical shielding layer can be used to shield the non-photosensitive portion of each pixel cell and thus minimize noise effects. An intermediate transfer gate and storage potential well can be incorporated to allow for the simultaneous integration of the array. Combined with the sensor's non-destructive readout capability, these supplemental gates make JPL's imaging device ideal for capturing faint objects.

A 32 x 27 active pixel sensor with a pixel size of 40 x 40 μm has been implemented in a 2- μm double-poly n-well CMOS process. The photogate voltage varied linearly with the amount of accumulated charge and no blooming was observed.



Plan view of a focal plane array suited for use with a column-parallel approach. Each pixel cell 15 in a column of the array is connected to a common load field effect transistor 65 and sampling circuit 70. The column-parallel array structure is read out by selecting an entire row using standard row and column select circuitry 18, 19 and outputting the read pixel values using a standard multiplexer 21.

APPLICATIONS

The technology has several potential applications:

Aerospace – guidance and navigation

Robotics – robot vision

PUBLICATIONS

U.S. Patent 6,943,838

More Information

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NP-2014-08-1139-HQ

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NPO-19621-1, NPO-19912-1, NPO-19117-1,
NPO-19581-1, NPO-19510-1, NPO-19246-1

